UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,761	07/26/2001	Jose Sanches	00GR01954248	7474

27975 7590 06/16/2004

ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER	
O BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	8

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,761	SANCHES ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 7/26/01, 9/21/01 and 1/16/02.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 20-59 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 20-59 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 January 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 20-59 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Pre-Amendment A as received on 7/26/01, IDS as received on 9/21/01, Declaration and Fee as received on 1/16/02, Priority Papers as received on 1/16/02 and Formal Drawings as received on 1/16/02.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

5. The title of the invention is not descriptive. It is simply a broad description of the field of the invention. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

6. Claims 20, 23-24, 29, 31, 35-36, 39, 41, 44-45, 48, 50, 54-55 and 58 are objected to because of the following informalities:

a. Claim 20 recites the limitations "N" and "I". However, it is unclear what the bounds on the values that "N" and "I" can attain. If they are negative, zero or fractional, the processor will not function with such a number of memory banks or instruction codes. Similarly, if "N" or "I" take on too great a number, the number of replicated execution units, or the number of instructions in one variable length instruction, could become infinite, again causing impossibly incorrect function. Please amend the claim language to more clearly point out the bounds of these quantities. Please correct similar problems in claims 23, 24, and 29, as well as corresponding claims 31, 35, 36, 39, 41, 44, 45, 48, 50, 54, 55, and 58, where new variables are defined without placing bounds on their values.

b. Claims 23, 35, 44 and 54 recite the limitations "I" as well as "i", the former representing the number of memory banks present, and the latter representing an i ranking memory bank. Please change one of the letters to a different letter to more clearly distinguish between the two letters more so than a capital versus lower-case letter does.

c. Claim 50 recites the limitation, "the signal processor" on its third line. There is insufficient antecedent basis for this limitation in the claim. Please correct the claim by providing the correct antecedent basis in the preamble, for example, "A method for reading variable-sized instructions in a signal processor".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 20-59 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claims 20, 32, 41 and 51 recite the limitation, "a program recorded in an interlaced fashion at a rate of one code per memory bank and per address applied to said memory banks". It is unclear how storing "one code per memory bank and per address" is a "rate", as "rate" is generally used in the context of a measurement with respect to time. Please correct the claim language to more clearly define the metes and bounds of the claimed invention. Dependent claims 21-30 and 42-49 are rejected for the same reasons as above, as they include the limitations of their parent claims.

10. Claims 20, 31, 41 and 50 recite the limitation, "comprises codes belonging to a following instruction". It is unclear from the claim language whether the reading means, a cycle, a number of codes, or something else entirely, comprises these codes that belong to a following instruction. Please correct the claim language to more clearly define the metes and bounds of the claimed invention. Dependent claims 21-30, 32-40, 42-49 and 51-59 are rejected for the same reasons as above, as they include the limitations of their parent claims.

11. Claims 20, 31, 41 and 50 recite the limitation, "with a cycle comprising at least one code to be read". It is unclear how a cycle can comprise "at least one code", as a cycle is generally used to refer to a measurement of time in which operations are performed. Please correct the claim language to more clearly define the metes and bounds of the claimed invention. . Dependent claims 21-30, 32-40, 42-49 and 51-59 are rejected for the same reasons as above, as they include the limitations of their parent claims.

12. Claims 24, 36, 45 and 55 recite the limitation, "c'(j) = c(i), and i +(j+R') modulo I". It is unclear whether the "and" is a logical AND operation between the results of the two sides of an expression, or whether it is simply a grammatical conjunction. Please correct the claim language to more clearly define the metes and bounds of the claimed invention. Dependent claims 25 and 26 are rejected for the same reasons as above, as they include the limitations of their parent claim.

13. Claims 24, 36, 45 and 55 recite the limitation "ranks of the codes" in its sixth line. There is insufficient antecedent basis for this limitation in the claim. Please correct the claim language to more clearly define and provide the correct antecedent basis for this claim. Dependent claims 25 and 26 are rejected for the same reasons as above, as they include the limitations of their parent claim.

14. Claims 24, 36, 45 and 55 recite the limitation, "c(i) designating i ranking codes in their arrangement after being read in said program memory". It is unclear what "after being read in" refers to, as it does not appear from the algorithm defined that anything is being "read into" the program memory. Please correct the claim language to more clearly define what the Applicant regards as the invention.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 20-21, 27-28, 31-33, 37-38, 41-42, 46-47, 50-52 and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraboschi et al., U.S. Patent No. 5,930,508, in view of Bratt et al., U.S. Patent No. 5,740,402.

17. Regarding claims 20, 31-32, 41, and 50-51, taking claim 20 as exemplary, Faraboschi has taught a signal processor for executing variable-sized instructions, each instruction comprising up to N codes (400 of Fig.4), the signal processor comprising:

a. A program memory (714 of Fig.7) comprising I individually addressable, parallel-connected memory banks with I being at least equal to N (see Col.5 line 61 – Col.6 line 7), said program memory comprising a program recorded in an interlaced fashion (see Col.7 lines 49-59),

b. Reading means for reading said program memory by reading a code in each of said I memory banks during a cycle for reading an instruction (see Col.5 line 61 – Col.6 line 7), with a cycle comprising at least one code to be read (see Col.5 line 61 – Col.6 line 7), and when a number of codes of the instruction read is less than I, comprises codes belonging to a following instruction (see Col.5 lines 12-25).

18. Faraboschi has not explicitly taught wherein the program is recorded in the program memory in an interlaced fashion at a rate of one code per memory bank and per address applied to said memory banks.

19. However, Bratt has taught the storing of consecutive instruction codes in consecutive memory banks in an interleaved fashion so that consecutive instruction codes can be read in parallel in a single cycle, thereby increasing the available memory bandwidth and allowing a VLIW processor to service each code in the instruction in parallel, thus increasing access time to the memory without adding more read ports (see Bratt, Col.1 lines 29-64). One of ordinary skill in the art would have recognized that it is desirable to not only increase the speed of a memory access, but to do so without adding additional hardware (read ports) that would otherwise have increased cost. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Faraboschi to store consecutive instruction codes in consecutive memory banks in an interleaved fashion so that the multiple instruction codes could be operated on in parallel, thus increasing the system throughput without adding additional hardware.

20. Claims 31-32, 41, and 50-51 are nearly identical to claim 20, differing only in claims 31-32 being embodied in a processor, claim 41 in a method for a processor, and claims 50-51 in a method for a signal processor, but all encompassing the same scope as claim 20. Therefore, claims 31-32, 41 and 50-51 are rejected for the same reasons as claim 20.

21. Regarding claims 21, 33, 42 and 52, taking claim 21 as exemplary, Faraboschi in view of Bratt has taught a signal processor according to claim 20, wherein said reading means comprises address means for applying to said memory banks individual addresses generated from a collective value of a program counter that is incremented (see Faraboschi, Col.4 lines 29-30),

before a beginning of the cycle for reading the instruction, by a value equal to a number of codes comprising a previous instruction (see Faraboschi, Col.2 lines 13-30). Here, while not taught explicitly, it is inherent that a read address be calculated before the cycle in which the read is performed, as without an address, the read cannot occur.

22. Claims 33, 42 and 52 are nearly identical to claim 21, differing only in claim 33 being embodied in a processor, claim 42 in a method for a processor, and claim 52 in a method for a signal processor, but all encompassing the same scope as claim 21. Therefore, claims 33, 42 and 52 are rejected for the same reasons as claim 21.

23. Regarding claims 27, 37, 46 and 56, taking claim 27 as exemplary, Faraboschi in view of Bratt has taught a signal processor according to claim 20, wherein said reading means comprises filtering means for filtering codes that do not belong to the instruction to be read, using parallelism bits accompanying the codes (see Faraboschi, Col.4 line 57 – Col.5 line 35).

24. Claims 37, 46 and 56 are nearly identical to claim 27, differing only in claim 37 being embodied in a processor, claim 46 in a method for a processor, and claim 56 in a method for a signal processor, but all encompassing the same scope as claim 27. Therefore, claims 37, 46 and 56 are rejected for the same reasons as claim 27.

25. Regarding claims 28, 38, 47 and 57, taking claim 28 as exemplary, Faraboschi in view of Bratt has taught a signal processor according to claim 27, wherein the filtered codes are replaced by no-operation codes (see Faraboschi, Col.7 lines 32-44).

26. Claims 38, 47 and 57 are nearly identical to claim 28, differing only in claim 38 being embodied in a processor, claim 47 in a method for a processor, and claim 57 in a method for a

signal processor, but all encompassing the same scope as claim 28. Therefore, claims 38, 47 and 57 are rejected for the same reasons as claim 28.

Allowable Subject Matter

27. Claims 22-26, 29-30, 34-36, 39-40, 43-45, 48-49, 53-55 and 58-59 are allowable over the prior art of record, but are rejected under 35 USC § 112 in above paragraphs 7-14. Further, claims 22-26, 29-30, 34-36, 39-40, 43-45, 48-49, 53-55 and 58-59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

28. The following is a statement of reasons for the indication of allowable subject matter:

a. Regarding claims 22, 34, 43, and 53, the prior art of record has taught circuitry which applies a separate address to each memory bank so that an entire VLIW instruction could be read from memory in a single cycle, wherein each address is determined using some significant bits of an address used to address the entire VLIW instruction (see Bratt, Col.1 lines 28-37). However, the prior art of record, or any combination of the prior art of record, has not taught wherein each separate address is determined of a division of the program counter by the number of memory banks. Claims 23, 35, 44 and 54 are also allowable over the prior art of record, as they are dependent upon claims with allowable subject matter.

b. Regarding claims 24, 36, 45 and 55, the prior art of record has taught a processor that has the ability to reorganize instruction codes in a memory in order to reduce wasted space in memory (see Faraboschi, Col.7 line 49 – Col.8 line 18).

However, the prior art of record, or any combination of the prior art of record, has not taught wherein the reorganization is performed according to the algorithm of claim 24, with rankings of the instruction codes before and after reorganization, and according to a remainder of a division of the program counter by the number of memory banks. Claims 25 and 26 are also allowable over the prior art of record, as they are dependent upon claims with allowable subject matter.

c. Regarding claims 29, 39, 48, and 58, the prior art of record has taught a processor which re-inserts NOP's into recently un-compacted instructions prior to execution based on instruction code locations in an alignment buffer which are empty (see Faraboschi, Col.7 lines 32-43). However, the prior art of record, or any combination of the prior art of record, has not taught wherein the filtering occurs according to the algorithm of claim 29, with ranking outputs of filtered instruction codes being defined according to a validation term associated with each ranking code. Claims 30, 40, 49 and 59 are also allowable over the prior art of record, as they are dependent upon claims with allowable subject matter.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

30. Hampapuram et al., U.S. Patent No. 5,787,302, has taught a variable length instruction format, with instructions stored in the compressed format in the memory and cache.

31. Vondran, Jr., U.S. Patent No. 6,480,938, has taught an instruction cache with multiple banks for use in holding variable length bundles of instructions.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
6/14/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100